PART A
(30 Marks)
(Question 1 is COMPULSORY and Answer EITHER Question 2 OR Question 3)

1. a) i) What is meant by a carry propagate adder? Give two examples of such adders.
(2 marks)

   ii) Compare them in terms of circuit complexity, speed of operation etc...
(4 marks)

   iii) Illustrate the difference in performance of an Arithmetic Right Shifter & a Logical Right Shifter
(2 marks)

b) i) Define the terms Architecture of a computer & Micro architecture. (2 marks)

   ii) Illustrate the difference between assembly language & Machine language. (2 marks)

   iii) What are the Instruction formats supported by MIPS Instruction Set? Illustrate using examples. (4 marks)

2 a) Translate the following R-type instruction into machine code.

   i)    add $s0, $s1, $s2
   ii)   addi $s0, $s1, 5
   (3 marks)  (3 marks)

b). Translate the following machine language code into assembly language.

   ox02F34022
   (4 marks)

c). Suppose that $s0 initially contains 0x23456789. After the following program is run on a big-endian system, what value does the ‘$s0’ contain? b) Consider the case in a little-endian system?

   sw $s0, 0($0)
   lb $s0, 1($0)
   (4 marks)

   OR

3 a) i) Explain how a fixed point number system is different from a floating point number system? (2 marks)

ii) Using manual methods perform the operation A x B and A / B on the 5-bit unsigned numbers A = 10101 and B = 00101.
(4 marks)

iii) Implement any one of the above operations using Hardware & explain it. (8 marks)
PART B
(30 Marks)
Question 4 is COMPULSORY and Answer EITHER Question 5 or Question 6

4a). Briefly explain the steps involved in program execution. (8 Marks)

b) i. What is the difference in operation of a single cycle & Multi cycle processor? (2)
   ii. Draw & explain the data path for an lw instruction in a Multi cycle processor. (6)

5. a). List the addressing modes of MIPS processor & explain each with an example (10)

   b) Show the MIPS instructions that implement the following pseudo instructions. You may use the assembler register, $at, but you may not corrupt (overwrite) any other registers.

      (a) addi $t0, $2, imm31:0
      (b) li $t5, imm31:0

   OR

6 a). Explain briefly the control unit of a single cycle processor. (4 marks)
   b). Determine the values of the control signals and the portions of the data path that are used when executing an ‘R type’ instruction. (10 marks)

PART C
(Marks : 40)
Question 7 is COMPULSORY and Answer EITHER Question 8 or Question 9

7 a. i). Explain briefly the different I/O accessing techniques. (3 marks)
   ii). Illustrate the different DMA transfer types & Modes. (5 marks)
   iii). What is Bus arbitration. Explain briefly. (2 marks)

   b. i). What are the parameters used to measure the performance of a memory system. Explain. (3 marks)
   ii. What are the different cache organizations? Explain w.r.t MIPS Memory system. (4 marks)

   iii). Consider the following case of a system with 2048 cache blocks and 8192 main memory blocks. Find where in the cache will the main memory blocks MMB-15 be placed for the mapping policies of: a) direct mapping, b) fully associative mapping, c) 4-way set associative. (3 marks)
8 a). Explain how reading & storing of data are performed in a DRAM cell and in a SRAM cell. (6 marks)

b). Explain why refreshing is essential in DRAMs & not needed in SRAMs. (4 marks)

c). Illustrate how the bit cells are arranged in a $4 \times 3$ memory array, & explain how to read data & store data in such an array. (8 marks)

d) Differentiate between single-ported & Multi-ported Memory. (2 marks)

OR

9. a). Define the term “Virtual Memory”. (2 marks)

b). Describe with suitable diagrams, how a logical address is converted to a physical address by a memory management unit. (12 marks)

c). What action will the MMU take if it finds that a requested segment is not present in physical memory? (4 marks)

d). What is the another major advantage of the indirect addressing provided by descriptor tables, besides the ability to address a large amount of virtual memory? (4)